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*****
;
; PROGRAM ID:      BOOTSTRAP INJECTION MODULE
;
; *****
;
; PROPERTY OF:     JADE COMPUTER PRODUCTS
;                  4901 W. ROSECRANS BLVD.
;                  HAWTHORNE, CALIFORNIA
;                  90250, U.S.A.
;
; *****
;
; VERSION:         2.2
;
; *****
; THE BOOTSTRAP INJECTION MODULE IS ONE OF TWO
; MODULES THAT TOGETHER MAKE UP THE SYSTEM RESIDENT
; BOOT. THIS MODULE IS DOWNLOADED INTO THE DOUBLE D
; MEMORY BY THE SYSTEM BOOTSTRAP DRIVER. THE MODULE
; THEN READS IN THE DISK CONTROLLER MODULE (DCM) FROM
; TRACK 0. THE ORIGIN OF THIS PROGRAM IS FIXED AS IT
; IS ASSEMBLED TO EXECUTE INSIDE THE DOUBLE D. THE
; BOOT INJECTION MODULE CAN THEREFORE RESIDE IN
; THE BOOTSTRAP PROM WITHOUT THE NEED TO REASSEMBLE.
; NOTE: STEP TIMING AND MOTOR TURN-ON DELAYS ARE
; DEFINED IN THIS MODULE. PATCHING MAY BE REQUIRED.
; ***** SK *****
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; *****
; CONTROLLER PORT ASSIGNMENTS
; *****

0000      BL.STS  ==      000H      ;BOARD STATUS
0000      BL.CTL  ==      000H      ;BOARD CONTROLS
0004      WD.CMD  ==      004H      ;1791 COMMAND REGISTER
0004      WD.STS  ==      004H      ;1791 STATUS REGISTER
0005      WD.TRK  ==      005H      ;1791 TRACK REGISTER
0006      WD.SEC  ==      006H      ;1791 SECTOR REGISTER
0007      WD.DTA  ==      007H      ;1791 DATA REGISTER
0008      XP.STP  ==      008H      ;STEPPER PULSE
0010      XP.MTO  ==      010H      ;MOTOR TIME OUT
0040      XP.MTX  ==      040H      ;MOTOR TIME EXTEND
0080      XP.DSH  ==      080H      ;DATA SYNC HOLD

; *****
; 1791-01 COMMAND CODES
; *****

0018      DC.HDL  ==      018H      ;LOAD R/W HEAD.
0090      DC.RMS  ==      090H      ;READ MULTI-SECTOR.
00D0      DC.STS  ==      0D0H      ;SET TYPE 1 STATUS.

; *****
; BOARD STATUS AND CONTROL PORTS
; *****

0001      BS.US0  ==      001H      ;1791-01 INDICATOR (CLOSED).
0000      BC.DR0  ==      000H      ;DRIVE 0 SELECT.
0004      BC.DSE  ==      004H      ;DRIVE SELECT ENABLE

; *****
; DISK STATUS MASKS
; *****

009C      DM.RER  ==      10011100B      ;READ ERROR TEST MASK
0004      DM.TK0  ==      00000100B      ;TRACK 0 TEST

; *****
; DISK DRIVE PARAMETERS
; *****

0008      TM.STP  ==      8              ;STEPPER INTERVAL - MS.
0001      TM.DBR  ==      1              ;DELAY BEFORE READ- MS.
0050      NB.TRK  ==      80             ;MAXIMUM NMBR OF STEPS.

; *****

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; *****
; INTERNAL MEMORY ASSIGNMENTS
; *****

0000 BANK.O == 0000H ; LOWER BANK ADDRESS.
0400 BANK.L == 0400H ; 1K BANK LENGTH.
0400 BANK.1 == BANK.O+BANK.L ; UPPER BANK ADDRESS.
0066 INT.NM == BANK.O+0066H ; NON-MASKABLE INT ADDR.
0376 BL.ERC == BANK.O+0376H ; ERROR CODE LOCATION.
0377 BL.DCS == BANK.O+0377H ; DISK CONTROLLER STAT.

; *****
; BOOTSTRAP COMMUNICATION
; *****

0001 BE.HOM == 001H ; HOME ERROR.
0002 BE.RDA == 002H ; READ ERROR A.
0004 BE.RDB == 004H ; READ ERROR B.

; *****
; DISK CONTROLLER MODULE (DCM) LINKAGE
; *****

000D DCM.SS == 13 ; FIRST DCM SECTOR = 13.
0403 DCM.BG == BANK.1+3 ; DCM COLD START ENTRY.
0400 DCM.LN == 0400H ; DCM LENGTH

; *****
; ASSEMBLER DIRECTIVES
; *****

.PABS ; ABSOLUTE ADDRESSING.
.PHEX ; INTEL HEX FILE FORM.
.XLINK ; NO LINKAGE OUTPUT.
0000 .LOC BANK.O ; PROGRAM START POINT

; *****
; DELAY MACRO. ALLOWS 1791 TO DIGEST INSTRUCTIONS
; *****

.DEFINE DELAY = [
    XTHL
    XTHL
    XTHL
    XTHL]

; *****

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*****
; SET STACK, START DRIVE MOTOR, AND SET INVERT SW (C) *
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0000 31 0400 BEGIN: LXI SP,BANK.1 ;SET UP STACK.
0003 DB40 IN XP.MTX ;TURN ON MOTOR.
0005 0E00 MVI C,0 ;ASSUME 1793.
0007 DB00 IN BL.STS ;INPUT STATUS.
0009 E601 ANI BS.USO ;TEST USER SW 0.
000B 2002 JRNZ SELECT ;GOTO SELECT DRV.
000D 0EFF MVI C,OFFH ;1791-01 INVERTS.
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*****
; CLEAR 1791-01 INTERRUPT AND SELECT DRIVE 0 *
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000F CD 009C SELECT: CALL STATUS ;179X-01 FORCED CLEAR.
0012 3E04 MVI A,BC.DSE!BC.DRO ;DRIVE 0, ENABLED.
0014 D300 OUT BL.CTL ;OUTPUT CONTROLS.
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*****
; POSITION R/W HEAD AT TRACK ZERO *
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0016 2E50 HOME: MVI L,NB.TRK ;SET MAX TRACKS.
0018 CD 009C STEP: CALL STATUS ;GET 179X STATUS.
001B E604 ANI DM.TKO ;TEST TRACK 0 BIT.
001D 200E JRNZ TRACK0 ;TRACK 0 EXIT.
001F 2D DCR L ;DEC ATTEMPTS.
0020 CA 0091 JZ ER.HOM ;CANT FIND TRK 0?
0023 DB08 IN XP.STP ;ISSUE STEP PULSE.
0025 11 0008 LXI D,TM.STP ;STEP INTERVAL TIME.
0028 CD 00A9 CALL TIMER ;PAUSE FOR PERIOD.
002B 18EB JMPR STEP ;TRY ANOTHER TIME.
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*****
; LOAD R/W HEAD ON SELECTED DRIVE *
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002D 79 TRACK0: MOV A,C ;GET TRACK 0 VALUE.
002E D305 OUT WD.TRK ;SET TRACK REGISTER.
0030 D307 OUT WD.DTA ;SEEK SAME TRACK.
0032 FD21 003D LXI Y,RD.SET ;SET NMI RETURN ADDR.
0034 3E18 MVI A,DC.HDL ;HEAD LOAD COMMAND.
0038 A9 XRA C ;INVERT (1791-01).
0039 D304 OUT WD.CMD ;ISSUE COMMAND.
003B 18FE JMPR . ;WAIT FOR INTERRUPT.
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; *****
; SET-UP FOR DCM READ OPERATION
; *****

003D 11 0001 RD.SET: LXI D, TM.DBR ; DELAY BEFORE READ.
0040 CD 00A9 CALL TIMER ; CALL MS. TIMER.
0043 11 0400 LXI D, BANK.L ; SET BANK LENGTH
0046 21 0400 LXI H, BANK.1 ; DCM LOAD ADDRESS
0049 FD21 0089 LXI Y, ER.RDA ; READ ERROR TRAP.
004D 3E0D MVI A, DCM.SS ; FIRST SEC OF DCM.
004F A9 XRA C ; INVERT (1791-01)
0050 D306 OUT WD.SEC ; SET 179X SEC REG.
0052 3E90 MVI A, DC.RMS ; READ MULTI-SECTOR.
0054 A9 XRA C ; INVERT (1791-01).
0055 D304 OUT WD.CMD ; ISSUE 179X COMMAND.
0057 E3 DELAY ; ALLOW 179X TO SETTLE.
005B 1813 JMFR R.BYTE ; GOTO READ ROUTINE.

; *****
; DISK INTERRUPT "NMI" ROUTINE
; *****

0066 .LOC INT.NM

0066 DB04 WD.INT: IN WD.STS ; GET 1791 STATUS.
0068 A9 XRA C ; INVERT (1791-01).
0069 32 0377 STA BL.DCS ; MAKE STATUS VISIBLE.
006C FDE3 XTIY ; EXCHANGE (SP)<>IY!
006E ED45 RETN ; BRANCH VECTOR ADDR.

; *****
; ACCEPT EACH BYTE AND STORE IN MEMORY
; *****

0070 DB80 R.BYTE: IN XP.DSH ; WAIT FOR DATA.
0072 DB07 IN WD.DTA ; INPUT INV DATA.
0074 A9 XRA C ; INVERT (1791-01).
0075 77 MOV M, A ; STORE DCM BYTE.
0076 23 INX H ; INCREMENT POINTER.
0077 1B DCX D ; DECREMENT LENGTH.
0078 7A MOV A, D ; GET HIGH REG.
0079 B3 ORA E ; THEN OR-IN LOW REG.
007A 20F4 JRNZ R.BYTE ; READ ANOTHER BYTE.

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; *****
; TEST READ STATUS, TERMINATE OPERATION, GO DCM
; *****

007C DB04 R.TEST: IN WD.STS ;INPUT READ STATUS.
007E A9 XRA C ;INVERT (1791-01).
007F E69C ANI DM.RER ;TEST FOR ERRORS.
0081 200A JRNZ ER.RDB ;READ ERROR TRAP.
0083 CD 009C CALL STATUS ;TERMINATE READ.
0086 C3 0403 JMP DCM.BG ;TRANSFER TO DCM.

; *****
; READ ERROR HAS BEEN DETECTED
; *****

0089 3E02 ER.RDA: MVI A,BE.RDA ;LOAD READ ERROR CODE.
008B 1806 JMPR ER.HLT ;GO TO ERROR HALT.
008D 3E04 ER.RDB: MVI A,BE.RDB ;LOAD READ ERROR CODE.
008F 1802 JMPR ER.HLT ;GO TO ERROR HALT.
0091 3E01 ER.HOM: MVI A,BE.HOM ;HOME ERROR CODE.
0093 32 0376 ER.HLT: STA BL.ERC ;DISPLAY ERROR CODE.
0096 AF XRA A ;ZERO A REG.
0097 D300 OUT BL.STS ;DESELECT DRIVE.
0099 DB10 IN XP.MTO ;MOTOR OFF!
009B 76 HLT ;TERMINATE.

; *****
; GET UPDATED 1791-01 STATUS
; *****

009C 3ED0 STATUS: MVI A,DC.STS ;TYPE 4 - STATUS.
009E A9 XRA C ;INVERT (1791-01).
009F D304 OUT WD.CMD ;ISSUE COMMAND.
00A1 E3 DELAY ;ALLOW 1791 TIME.
00A5 DB04 IN WD.STS ;GET STATUS
00A7 A9 XRA C ;INVERT (1791-01).
00A8 C9 RET ;RETURN TO CALLER.

; *****
; TIMER - WAIT FOR (BC * 1.0) MILLISECONDS
; *****

00A9 3EF7 TIMER: MVI A,247 ;LOAD INT MS VALUE.
00AB 3D MS.INT: DCR A ;DEC FOR 1 MS.
00AC 20FD JRNZ MS.INT ;REPEAT FOR 1 MS.
00AE 1B DCX D ;TEST FOR ANOTHER MS.
00AF 7A MOV A,D ;CHECK REG D.
00B0 B3 ORA E ;AND REGISTER E.
00B1 20F6 JRNZ TIMER ;DO ANOTHER 1 MS.
00B3 C9 RET ;TIME PERIOD EXPIRED!

; *****

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.END

BANK.0 0000	BANK.1 0400	BANK.L 0400	BC.DRO 0000
BC.DSE 0004	BEGIN 0000	BE.HOM 0001	BE.RDA 0002
BE.RDB 0004	BL.CTL 0000	BL.DCS 0377	BL.ERC 0376
BL.STS 0000	BS.USO 0001	DCM.BG 0403	DCM.LN 0400
DCM.SS 000D	DC.HDL 0018	DC.RMS 0090	DC.STS 00D0
DM.RER 009C	DM.TKO 0004	ER.HLT 0093	ER.HOM 0091
ER.RDA 0089	ER.RDB 008D	HGME 0016	INT.NM 0066
MS.INT 00AB	NB.TRK 0050	RD.SET 003D	R.BYTE 0070
R.TEST 007C	SELECT 000F	STATUS 009C	STEP 0018
TIMER 00A9	TM.DBR 0001	TM.STP 0008	TRACK0 002D
WD.CMD 00C4	WD.DTA 0007	WD.INT 0066	WD.SEC 0006
WD.STS 00C4	WD.TRK 0005	XP.DSH 0080	XP.MTO 0010
XP.MTX 0040	XP.STP 0008		

1. The first part of the book is devoted to a discussion of the history of the theory of the firm. It begins with a survey of the classical theory of the firm, which is based on the assumption of perfect competition and perfect information. This theory is then contrasted with the modern theory of the firm, which is based on the assumption of imperfect competition and imperfect information. The modern theory of the firm is then developed in a series of chapters, each of which deals with a different aspect of the theory.	2. The second part of the book is devoted to a discussion of the theory of the firm in the context of the theory of the market. It begins with a survey of the classical theory of the market, which is based on the assumption of perfect competition and perfect information. This theory is then contrasted with the modern theory of the market, which is based on the assumption of imperfect competition and imperfect information. The modern theory of the market is then developed in a series of chapters, each of which deals with a different aspect of the theory.
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